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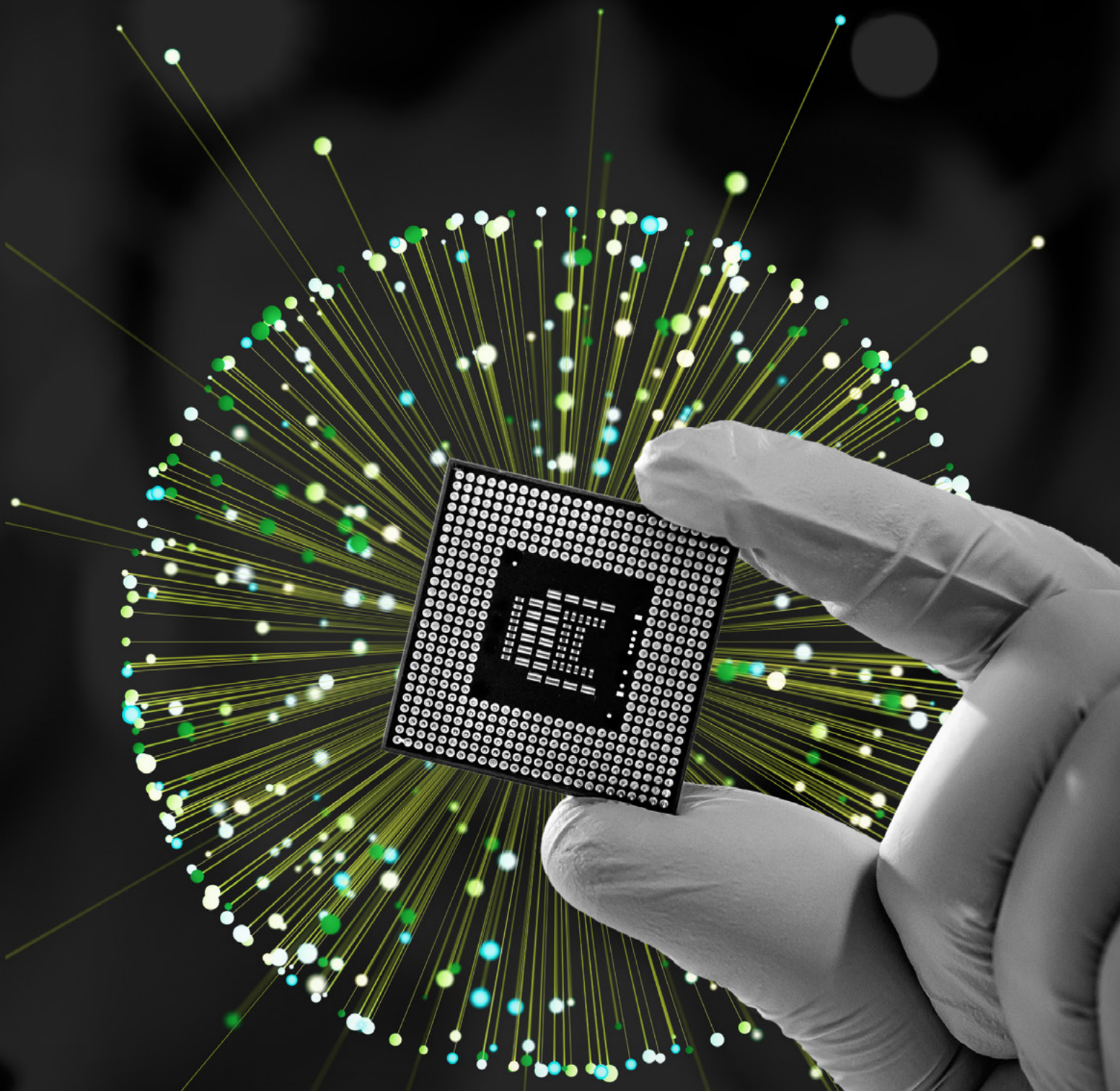
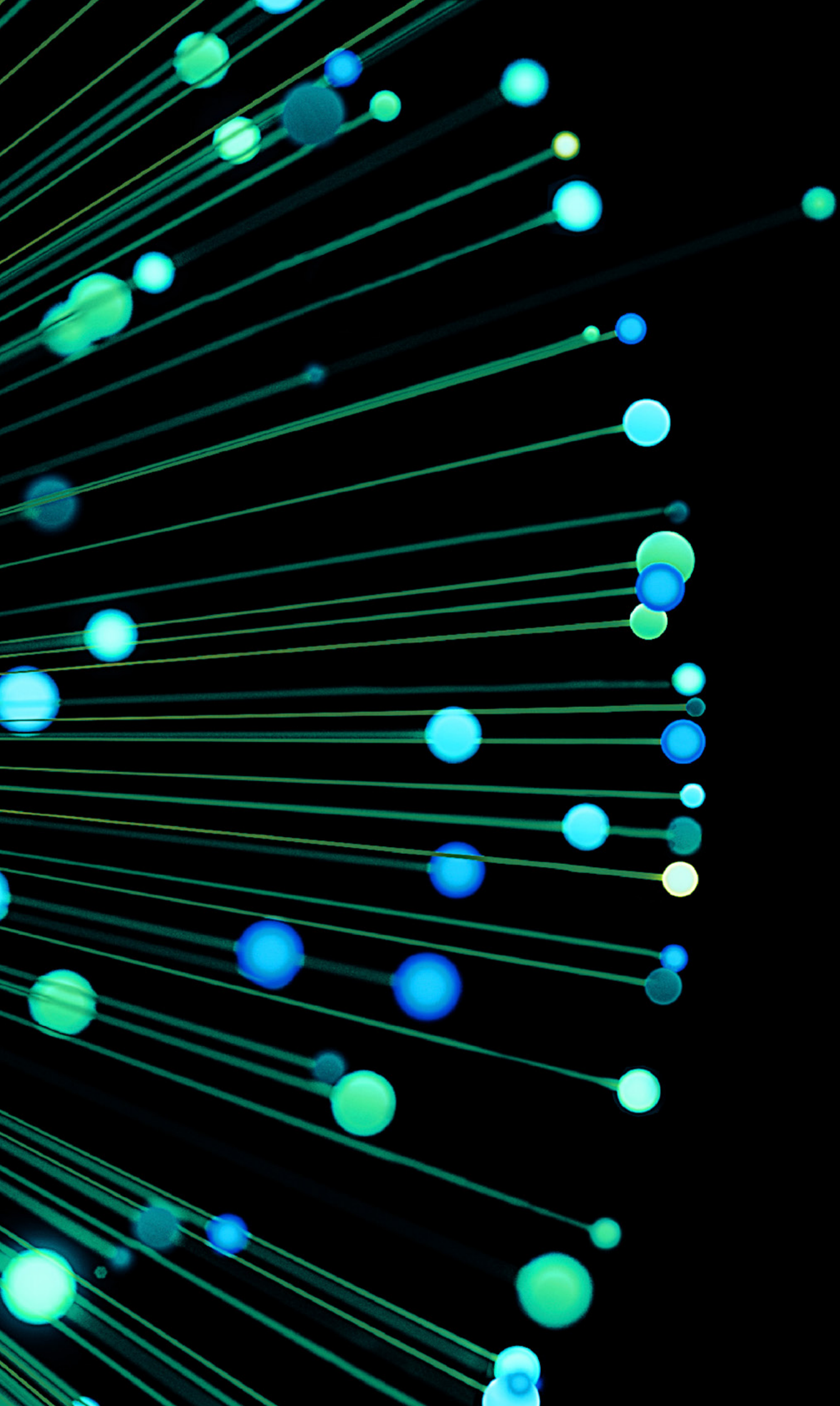


Semiconductor – A treasure trove for private equity investors

Deloitte Private Equity

A greater return on ideas

June 2024



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Deloitte Private Equity

A greater return on ideas

www.deloitte.com/privateequity

Our Private Equity Leaders

Global
Emma Cox
ejcox@deloitte.co.uk

EMEA
Karsten Hollasch
khollasch@deloitte.de

Asia Pacific
Satoshi Sekine
satoshi1.sekine@tohmatsu.co.jp

United States
Bryant Huber
mehuber@deloitte.com

United Kingdom
James Clare
jclare@deloitte.co.uk

Asia Pacific
Dwight Hooper
dwhooper@deloitte.com.hk

Canada
Mark Jamrozinski
mjamrozinski@deloitte.ca

Semiconductor – A treasure trove for private equity investors

Ample investment opportunities

The semiconductor industry is a significant powerhouse within the global economy, underpinning the technological advancements that shape our contemporary world. As the essential building blocks of electronic devices, semiconductors play a pivotal role in a vast array of sectors, driving innovation and productivity in everything from consumer electronics to sophisticated industrial systems. Semiconductors accounted for around US$520 billion in sales last year, with various forecasts predicting it will be a trillion-dollar industry by 2030.

The semiconductor industry is experiencing profound changes presenting various investment opportunities for private equity investors attuned to the industry's evolving landscape. Already an industry many private equity firms have made (limited) strategic investments in, significant opportunities arise from trends such as the advent of chiplets, the rise of AI-specific semiconductor developments, specialized AI downstream models, and the disruption through AI-based design techniques.

Each trend offers unique entry points for strategic investments that can yield significant returns. Even for those investors that do not want to invest directly into semiconductor companies, opportunities are paramount through investing in the semiconductor supply chain. At a time that public sector engagement with semiconductors increases across the globe, at the very least it warrants a fresh look at this high-growth industry.

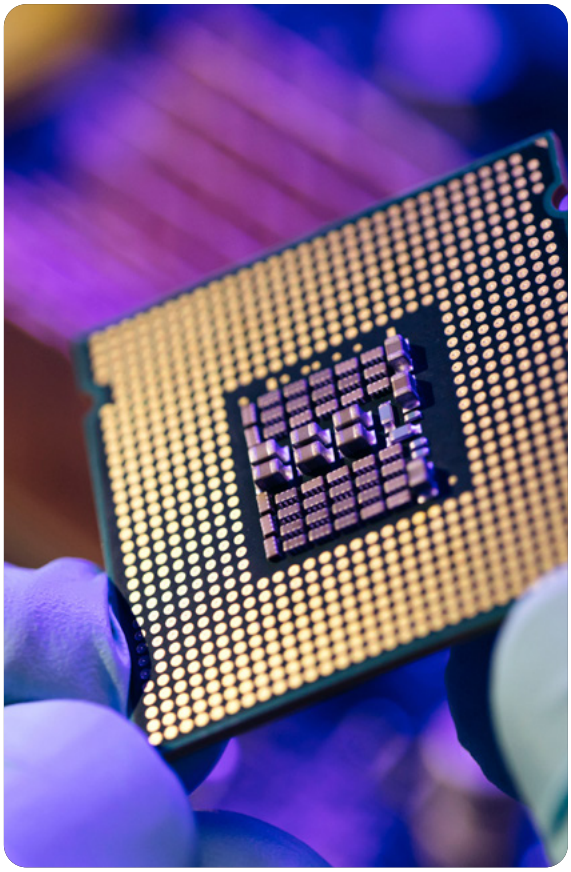
01
Capitalizing on chiplet innovation

The semiconductor industry faces challenges in high-end semiconductors, especially as AI and other architectures require different components like CPUs, GPUs, and memory to be on the same chip.

This poses two fundamental issues: the increased probability of defects as chip sizes grow, and the ever-increasing complexity of different fabrication and packaging technologies for different components.

To tackle these challenges, chiplets have emerged as a solution. Chiplets enable the creation of a large chip by integrating multiple smaller chiplets, reducing the probability of defects and improving yield and cost efficiency. This approach allows for the integration of diverse functional blocks onto a single chip, enabling both increased functionality and efficiency for semiconductors, known as "More than Moore".

Investment perspective: Chiplet technology unlocks a wealth of opportunities across the semiconductor value chain, ranging from standardized interconnect techniques, intellectual property (IP) and electronic design automation (EDA), to fabless manufacturing, foundries, and advanced packaging and testing. By investing in this sphere, private equity firms can harness the momentum of a market poised for growth and innovation, positioning themselves at the forefront of industry partnerships and alliances.



02

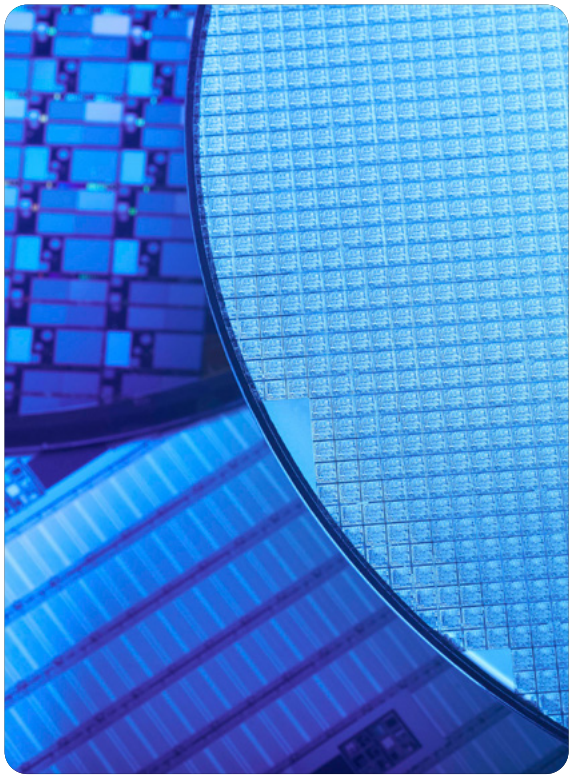
AI specific semiconductor developments and innovations

AI-specific semiconductor developments and innovations have intensified competition with new entrants, with AI making a fundamental impact on both the core (e.g., computing and network) and the edge (e.g., device and sensors).

As AI is embedded in the core, there is a shift from training to inferencing, creating opportunities for new architectures optimized for AI neural networks. Startups and hyperscale companies experiment with innovative chip designs to challenge incumbents and optimize the overall AI system.

On the edge, large language models (LLMs) are integrated into Systems on Chip, merging AI and sensors to provide "intelligent vision on the edge". As an example, number plate recognition is performed on chips, reducing network traffic and central processing needs, creating new low-cost intelligent endpoints.

Investment perspective: Private equity investors can leverage growth in AI-centric semiconductor design and engineering by targeting specialized IP blocks that amplify AI capabilities. Investment in startups and scaling solutions into industry verticals can exploit AI's transformative potential across the board.



03

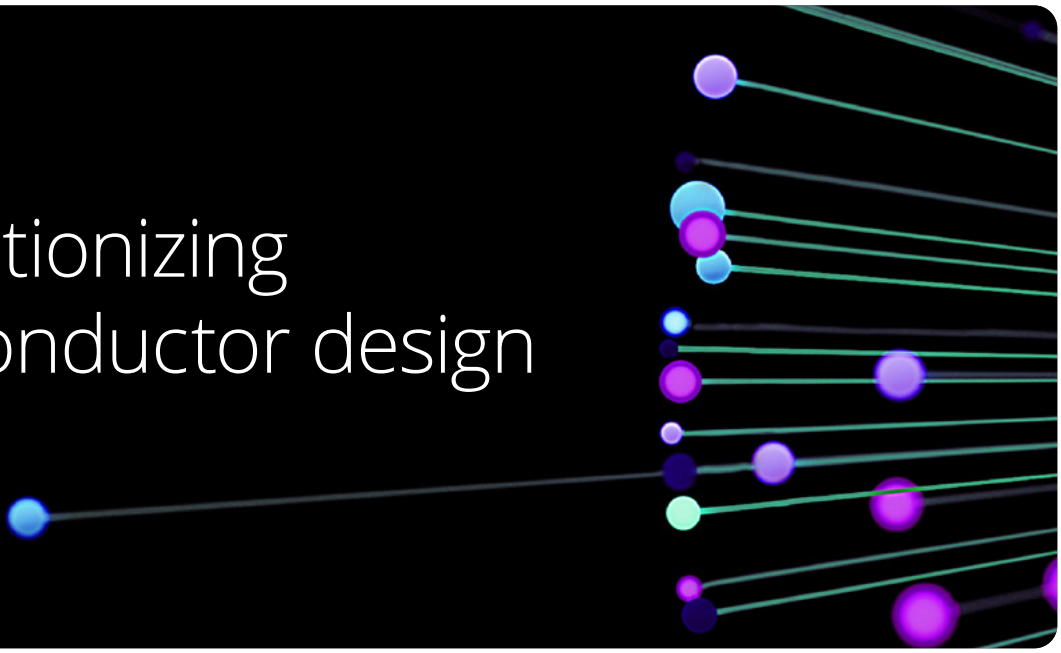
The emergence of AI-oriented datacenters-AI specific downstream models

The rise of AI also significantly influences the data center industry, leading to the design of "AI Factories".

Power density and total power requirements are increasing significantly, leading to optimized layouts, as well as new thermal and cooling designs. Network connectivity between nodes and to the outside can be optimized. Integration as with chiplets is replicated at the data center level to yield end-to-end optimization.

Investment perspective: The evolving datacenter landscape and the need for specialized AI services present lucrative investment avenues for private equity. By focusing on datacenter infrastructure tailored to AI and emergent AI service providers, investors can seize a substantial market share and lead the way for "AI-as-a-service" models.

04 Revolutionizing semiconductor design (by AI)



AI does not only transform the applications requirements for semiconductors but also disrupts the semiconductor design process. Amidst increasing customer demand, there is immense pressure to develop and supply ever-more-complex semiconductors ever-faster.

The emergence of Gen AI is enabling the industry to innovate at an accelerated pace, delivering more capable and efficient chips and maintaining quality.

According to Deloitte's survey on SEMI, Gen AI adoption for semiconductor design, including verification, validation, and physical design, is recognized as the area with significant potential. Semiconductor giants invested approximately US$300 million in AI tools for chip design in 2023, a total expected to rise to US$500 million by 2026. And 72% of the semiconductor professionals Deloitte polled in 2023 believe that GenAI's impact on the industry will be high to transformative.

"While embracing AI-based design offers immense possibilities, it is crucial to carefully consider factors like costs, accuracy, bias, and privacy to manage associated risks effectively."

Investment perspective: As GenAI-based design methodologies redefine semiconductor creation, private equity firms have the opportunity to back scale-ups in this domain, ensuring profitable exits through established EDA companies and design houses.

Investors must recognize the interdependent nature of the semiconductor supply chain, where strategic partnerships and corporate venturing are key to fostering innovation. Utilizing venture client solutions, such as those provided by companies like 27 pilots, allows for the scaling of startups and the cultivation of an innovation ecosystem, granting investors a competitive edge.

05

Highly specialized supply chain, with no margin for error

With semiconductor companies finding solutions for some of the worlds most complex problems there is another angle for private equity investors to consider. In order to be able to produce these highly sought after chips there is a very active and growing specialized supplier base.

Key elements of the typical supplier to a semiconductor company are amongst others supreme and consistent quality (no tolerance for errors), ability to scale at pace (in line with sudden demand shifts), high drive to innovate and working together in a complex landscape where some competitors in one end market have to work together in order to seamlessly operate in the semiconductor supply chain.

Investment perspective: In order to scale at pace and to keep track with semiconductor companies that typically have a global footprint, the supplier landscape is professionalizing and growing.

With more companies co-developing certain solutions with semiconductor companies in their own area of expertise (e.g., high-precision machining, clean room solutions, factory automation).

"Helping suppliers grow at pace is an opportunity and task that private equity is most suited for, either in support of the current entrepreneur or by driving growth in the company's next evolutionary phase."

Deep dive: Chiplets

The issue in high-end semiconductors: AI and other architectures require ever-larger (in mm²) sizes of different components like CPU, GPU and memory in close proximity (close–in µm)–meaning on the same chip.

That brings, allowing for some simplification, two problems–(1) the larger the chip area, the higher the probability of a defect and (2) memory, CPU, GPU are produced in different fab technologies. Monolithic fabless (e.g., AMD, NVIDIA) and IDMs (e.g., intel) have therefore long introduced multi-die-systems–making a large chip from multiple chiplets and integrating them into one package, using a wide range of interconnection techniques. Thus, Moore's law can extend: "more Moore" or "SysMoore" (Cambrian AI Research: Art de Geus - Sysmoore, 2021). While it has become harder to shrink structures, moving or stacking chiplets closer together allows you to push integration densities further.

In hybrid semiconductors at lower node density, development is the same motivated by the need to integrate ever more diverse functional blocks in a single package, for example, a sensor, its intelligent "edge" signal processing and say networking functionality. Different functions, made with different fab processes require again chiplets as a solution. This does not bring higher density, but richer diversity of functionality on a single chip "more than Moore".

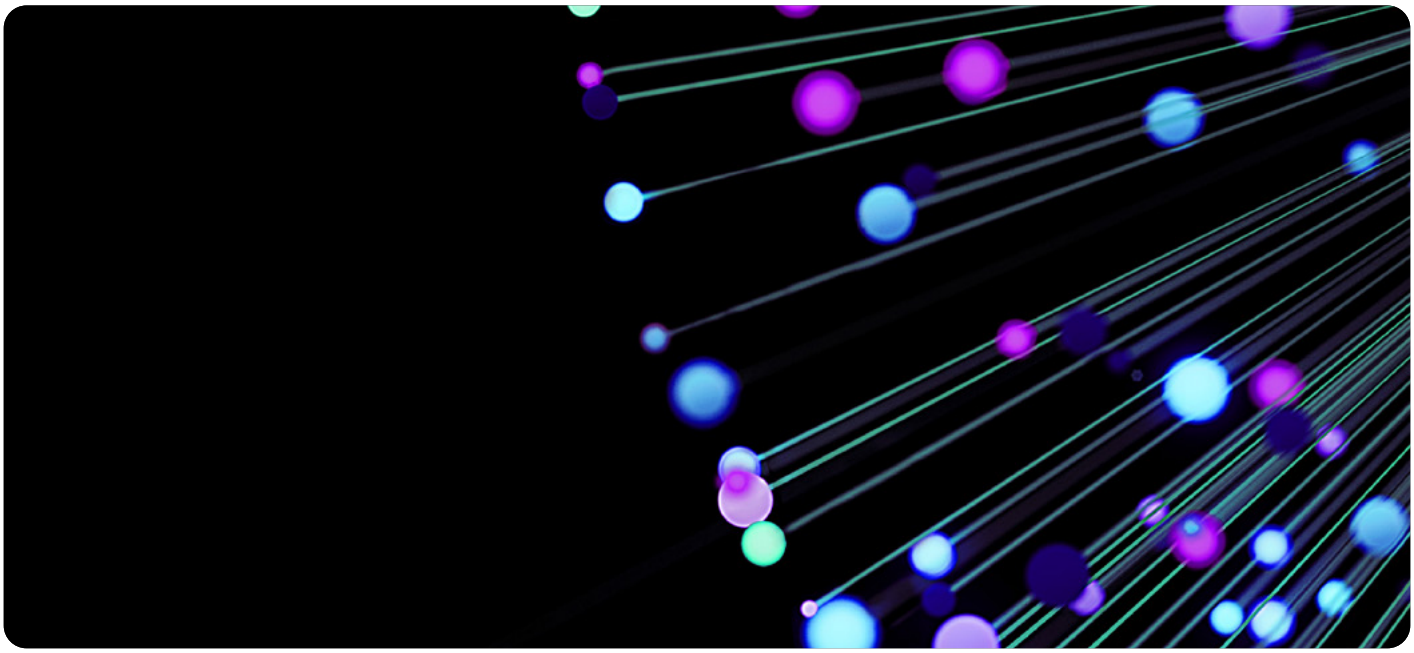
In other words, **chiplets fundamentally enable the main development vectors for semiconductors**.

This trend is not without challenge. Upstream in the value chain (IP and design tools), new design and simulation tools must embrace the system complexity of hybrid chips and their interconnection. More granular simulation must consider thermal effect of power dissipation, the physical connection properties between chiplets and interactions with the substrate holding the chiplets in place. For IP vendors, the chiplet as a point of modularity will gain more prominence to delineate their solutions.

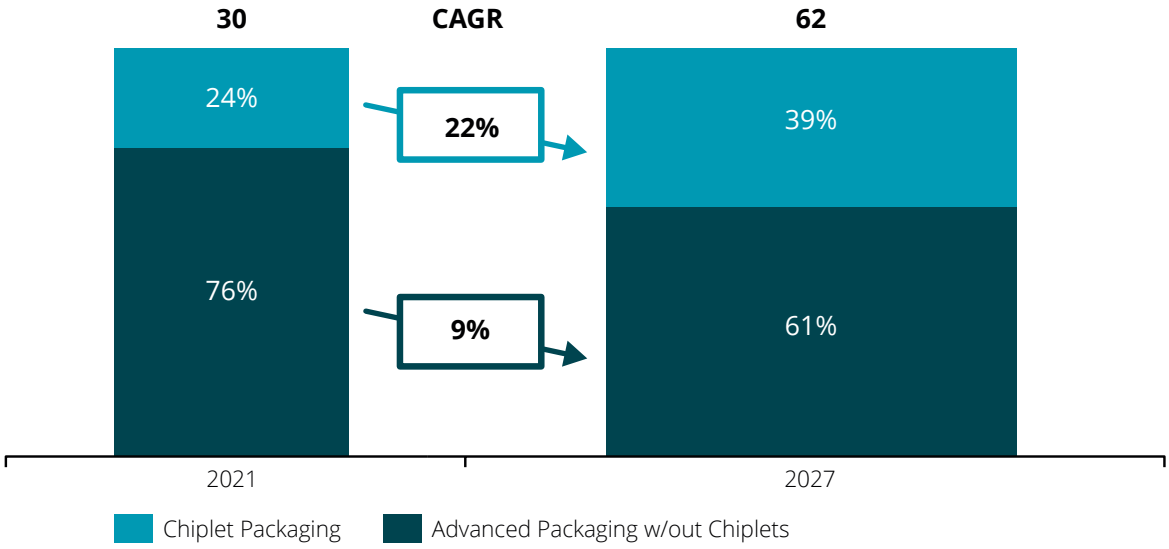
Downstream in the value chain, packaging becomes the next battlefield after EUV pushed frontend manufacturing to its current capability. Usage of advanced packaging for the express use in chiplet packing is expected to grow at a 7% CAGR between 2021 and 2027. (Graph 1)

Packaging and chiplet interconnect (IX) is a highly diverse field, with standards like UCIe evolving, while each packager or, fab-packager alliance, has devolved proprietary technologies.

In summary, it is fascinating to see how a bottleneck in frontend manufacturing pushes the adjacent semiconductor value chain steps to become more innovative and flexible, giving rise to more complex semiconductor systems.



Advanced packaging market share (US$, billion) (%) by usage with and without chiplets



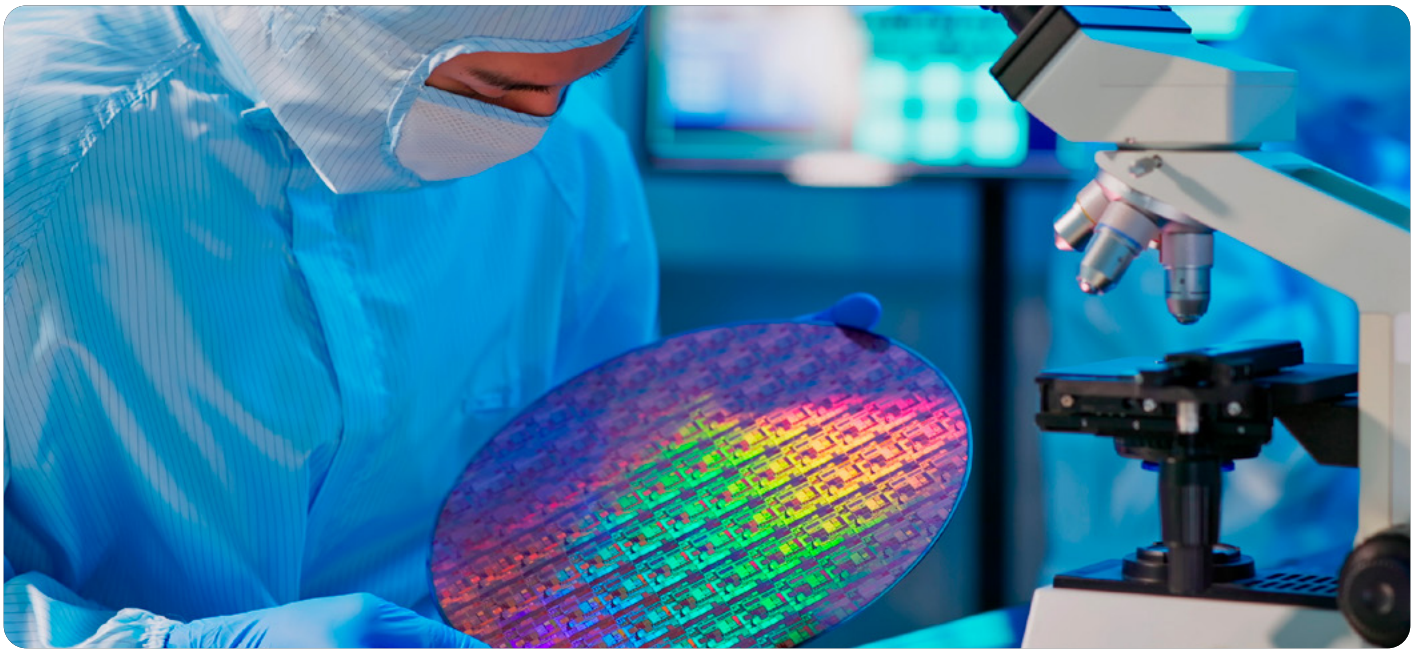
Source: Global Market Stats and Figures, Monitor Deloitte Analysis

Chiplets are not new to IDM and fabless vendors. The next exciting step of this development is currently unfolding: A market of standardized chiplets will enable system engineering to combine/build custom chips from chiplet components. With chiplets going mainstream, the need for more standardized chiplet interconnect techniques arises.

Further changes are in testing where dies must be verified known good dies before being placed onto the substrate with other chiplets. Similarly, standardized data platforms that connect the entire ecosystem from design to packaging become ever more important, both allowing to combine and protect the IP from different IP vendors.

End customers can decide whether to build their own chips/chiplets. They need to build capability (and capability at the right scale) and consider if they generate enough volume per custom design.

Will third parties orchestrate the value chain for the end customers going into chiplet design? Or will this be a fab/packaging/EDA play?



In summary, new venture opportunities, business models and transformation challenges arise (with references which prove the assertion):

IP: Design and market end-to-end encapsulated IP in chiplets (Nvidia's GPU Chiplet Design Unlocks Potential in Emerging Markets, 2023)

EDA: Enhance design and simulation for hybrid semiconductor systems

Fabless: Consider the IP model above and offer e.g., AI modules to third parties

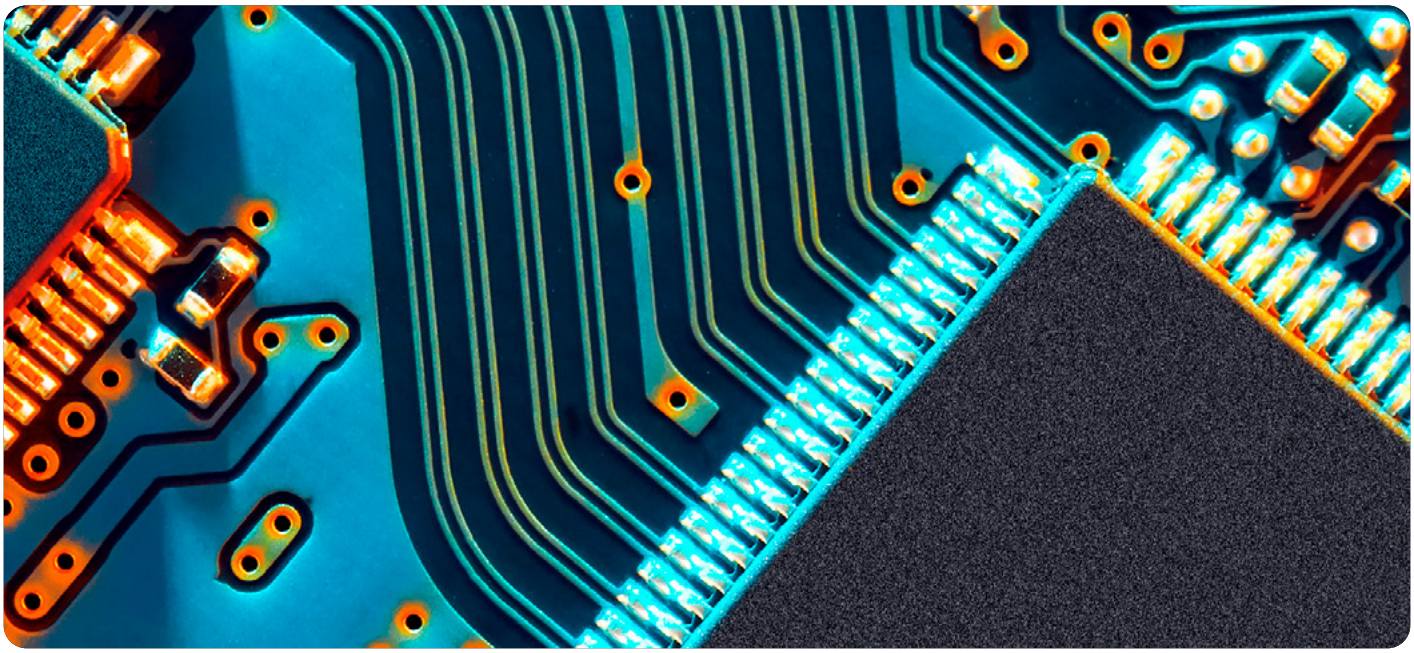
Fabs: Strengthen packaging alliances or build organic packaging skills and standards, continuously add capacity

Packaging: Scale up complex packaging processes and create value-add IX strategy

Testing: Adjust testing process and tools to work at chiplet and system levels

New plays and alliances: Organic growth and M&A for engineering firms to integrate multivendor chiplets; standards, initiatives and alliances for chiplets to interconnect

It is amazing to see how approaching limitations in frontend manufacturing have pushed innovation upstream and downstream. Investors can capitalize on investing into startups which adeptly navigate and innovate around these innovations and unlock the true value and potential of chiplets.



Advantages and challenges of chiplets through the value chain

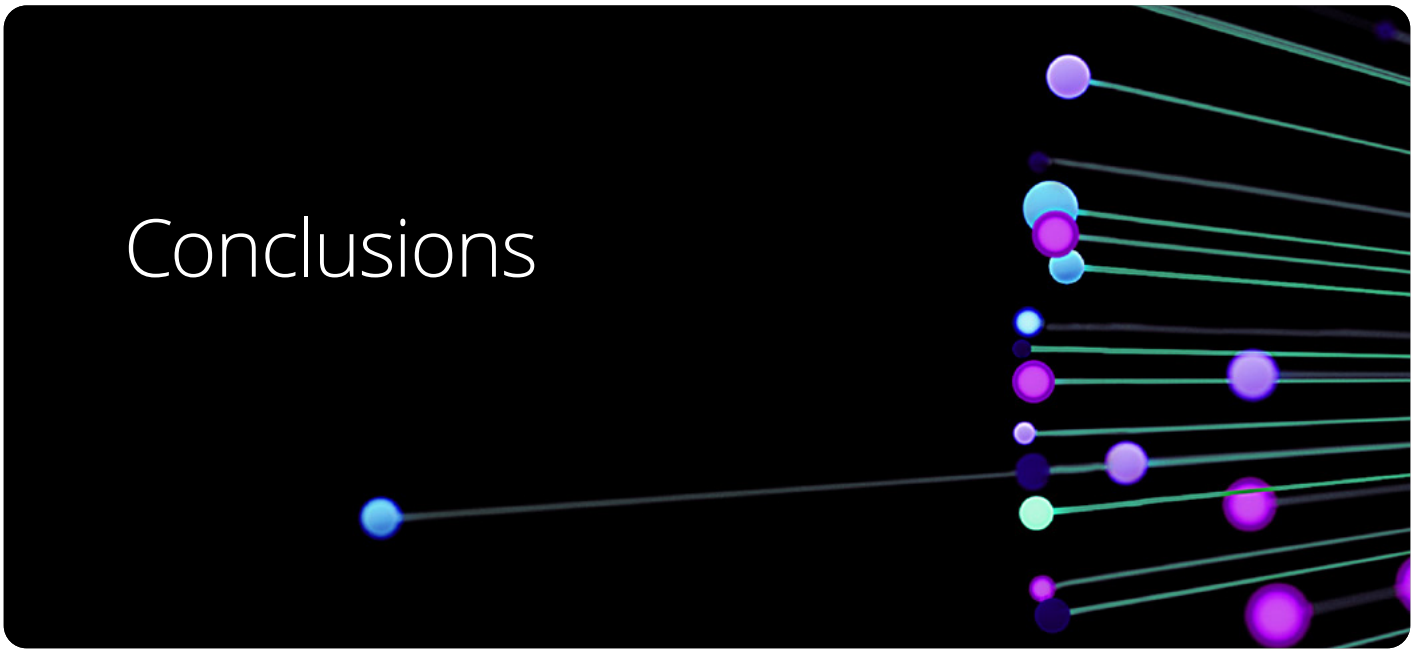
Intellectual Property
An IP-block is the functional block of a chip design that can be used many times

Wafers
Equipment
Material and chemicals

	Electronic Design Automation (EDA)	Design	Manufacturing (frontend)	Assembly, packaging and testing (or back-end manufacturing)	End-product integration
Advantages	Break Design into multiple logical and functionally **separate building blocks** **Use different IP sources** in their native technology / node	**Modularity:** re-use of existing designs for new use cases, simplified versioning Go beyond the reticle limit **Shortened low-level design time** **Greater confidence** in **hitting application specifications**	**Higher yield** due to smaller chiplet area (mm), more known good dies **Improved wafer utilization** at the edges –greater die area per wafer **Standardization for higher volumes** of core chiplets reduces production costs	New ways to **differentiate packaging** offers for multivendor chiplets Packaging moves from "utility function" to **differentiating enabler**	**Less over-specification and/or better fit to purpose** as chiplets reduce costs by enabling mixing and matching of dies from leading and mature nodes. Customers **can influence system design** by combining multiple chiplets, and **introduce limited customization**
Disadvantages	**Increased complexity** in the management of chip-level connectivity **Finer granular simulation** required for e.g. power management **Little design support** (particularly for ODSA's BoW and Open HBI interfaces) **No standards** for chiplets in EDA tool flows	**New tool chain needed** to integrate multiple EDA tools/environments for multiple chiplets **Complex integration** between chiplets on substrate **Lack of design support** for some die-to-die interconnect schemes	**Expansion of guard bands** required to ensure consistent ensure adherence to industry standards e.g."known good die" standard **More complex end-to-end MPS** generation **More sophisticated planning optimizer required** to achieve expected OEE	**Exponentially increasing packaging complexity** **Significant technical and cost challenges** to test and probe chiplets **Upskilling of package designers** required **Ensuring integrity and secure procedures** due to decentralised manufacturing processes	**Many chiplet Interface protocols** with no industry defined standard Rise of **chiplet integration as an additional engineering** skill

Source: Advanced Packaging, Statistica, anysilicon, Semiconductor Engineering, Monitor Deloitte Analysis

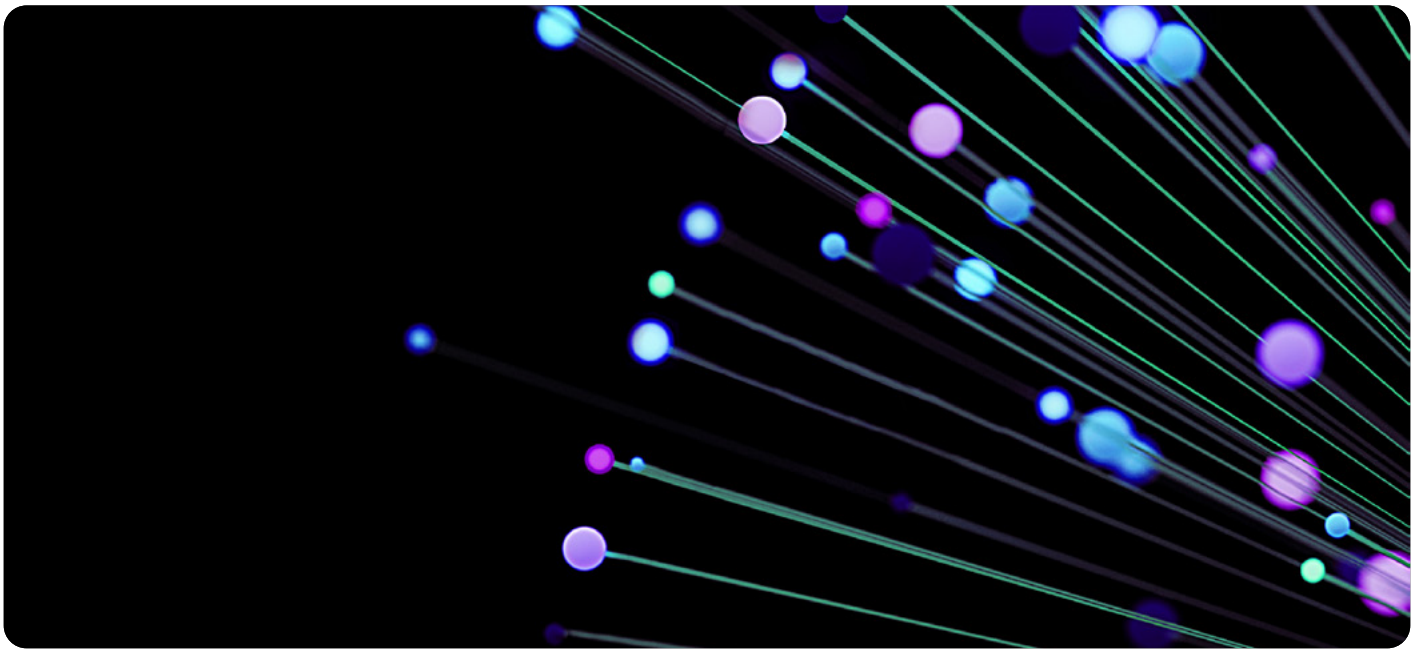
Conclusions



The semiconductor industry's significance to the global economy and its trajectory of exceptional growth cannot be overstated. This industry remains at the heart of most, if not all, technological advancements that shape our contemporary world.

AI and the restructuring of the value chain, embracing an end-to-end system perspective, create additional market opportunities. The time to invest is, therefore, now. Private equity has a spectrum of opportunities to engage with and contribute to this dynamic sector. Funding opportunities, like promising innovations to acquiring and optimizing existing enterprises and investing in the supply chain provide expansion capital, each with a variety of risk/return profiles.

With generous capital injections on the horizon from both government entities and industry players, a unique range of partnering and exit opportunities arises. As the semiconductor industry continues to evolve and expand, private equity investors are well-positioned to not only reap the financial rewards but also to foster the next wave of semiconductor development.



Authors

Dr. Uwe Lambrette
Partner, EMEA Semiconductor Lead, Deloitte Consulting GmbH

ulambrette@deloitte.de
+49 151 12683211

Dieter Trimmel
Partner, Private Equity TMT Industry Lead, Deloitte Consulting GmbH

dtrimmel@deloitte.de
+49 151 18294000

Roën Blom
Partner, Private equity, TMT Due Diligence Lead, Deloitte Financial Advisory BV

rblom@deloitte.nl
+31 882885752

Haruka Konno
Senior Consultant, Semiconductor practice, Deloitte Consulting GmbH

hkonno@deloitte.de
+49 21187728861

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